WHAT IS CLAIMED IS:

1. An electrical integrity testing apparatus for testing electrical integrity of nets on a circuit under test, comprising:

a stimulating probe couplable to a first end of a net of interest on said circuit under test;

a signal generator couplable to said stimulating probe operable to generate a known signal;

a capacitive sensing probe operable to capacitively couple a signal from a second end of said net of interest when said known signal stimulates said first end of said net of interest; and

a signal correlator which performs signal correlation on a digital representation of said capacitively coupled signal with said known signal based only on said capacitively coupled signal and an expected digital signature of said known signal.

2. An apparatus in accordance with claim 1, comprising:

a classification function responsive to correlation results generated by said signal correlator to classify said net of interest into one of a plurality of different levels of conductive integrity.

3. An apparatus in accordance with claim 1, further comprising:

a filter which filters signal components from said capacitively coupled signal outside a predetermined frequency range, said predetermined frequency range comprising at least a range of frequencies of said known signal.

4. An apparatus in accordance with claim 1, wherein said known signal comprises a coded pulse-train sequence and said signal correlation comprises cross-correlation of said digital representation of said capacitively coupled signal with an expected digital signature of said coded pulse-train sequence.

5. An apparatus in accordance with claim 1, wherein said known signal comprises a square-wave pulse train and said signal correlation comprises auto-correlation of said digital representation of said capacitively coupled signal with itself.

6. An apparatus in accordance with claim 1, wherein said known signal comprises a square-wave pulse train and said signal correlation comprises cross-correlation of said digital representation of said capacitively coupled signal with an expected digital signature of said square-wave pulse train.

7. An electrical integrity testing apparatus for testing electrical integrity of a plurality of nets on a circuit under test, comprising:

a plurality of stimulating probes each couplable to a respective first end of a corresponding net of interest on said circuit under test;

a plurality of signal generators each corresponding to one of said plurality of stimulating probes and operable to generate a respective known signal on said respective stimulating probe;

a plurality of sensing probes each corresponding to one of said plurality of stimulating probes and operable to sense a signal from a second end of said net of interest when said respective known signal stimulates said first end of said corresponding net of interest; and

a signal correlator which performs signal correlation between each of said respective sensed signals and said respective known signals.

8. An apparatus in accordance with claim 7, comprising:

a classification function responsive to said signal correlator to classify each of said respective nets of interest into one of a plurality of different levels of conductive integrity.

9. An apparatus in accordance with claim 7, wherein:

at least one of said plurality of sensing probes comprises a capacitive sensing probe which capacitively senses said respective sensed signal.

10. An apparatus in accordance with claim 7, further comprising:

a plurality of filters each corresponding to one of said plurality of stimulating probes and operable to filter signal components from said respective sensed signal outside a respective known frequency range, said respective known frequency range comprising at least a range of frequencies of said respective known signal.

11. An apparatus in accordance with claim 7, wherein at least one of said respective known signals that stimulate a respective first end of a respective net of interest comprises a coded pulse-train sequence and said signal correlation comprises cross-correlation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with an expected digital signature of said coded pulse-train sequence.

12. An apparatus in accordance with claim 7, wherein at least one of said respective known signals that stimulate a respective first end of a respective net of interest comprises a square-wave pulse train and said signal correlation comprises auto-correlation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with itself.

13. An apparatus in accordance with claim 7, wherein said known signal comprises a square-wave pulse train and said signal correlation comprises cross-correlation of said digital representation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with an expected digital signature of said square-wave pulse train.

14. An electrical integrity testing apparatus for testing electrical integrity of nets of interest on a circuit under test, comprising:

a plurality of stimulating probes each couplable to a respective first end of a corresponding net of interest on said circuit under test;

a plurality of signal generators each operable to generate a respective known signal on a respective signal generator output;

a signal generator configuration controller operable to couple said plurality of signal generator outputs of said plurality of signal generators to respective stimulating probes in a one-to-one mapping;

one or more sensing probes each corresponding to a subset of said plurality of stimulating probes and operable to sense a respective signal from a respective second end of each of said nets of interest corresponding to said subset of said plurality of stimulating probes when said respective known signal applied to said respective stimulating probe stimulates said first end of said corresponding net of interest; and

a signal correlator which performs signal correlation between each of said respective sensed signals and each of said corresponding respective known signals.

15. An apparatus in accordance with claim 14, comprising:

a classification function responsive to said signal correlator to classify each of said respective nets of interest into one of a plurality of different levels of conductive integrity.

16. An apparatus in accordance with claim 14, wherein:

at least one of said plurality of sensing probes comprises a capacitive sensing probe which capacitively senses said respective sensed signal.

17. An apparatus in accordance with claim 14, further comprising:

a plurality of filters each corresponding to one of said plurality of stimulating probes and operable to filter signal components from said respective sensed signal outside a respective known frequency range, said respective known frequency range comprising at least a range of frequencies of said respective known signal.

18. An apparatus in accordance with claim 14, wherein at least one of said respective known signals that stimulate a respective first end of a respective net of interest comprises a coded pulse-train sequence and said

signal correlation comprises cross-correlation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with an expected digital signature of said coded pulse-train sequence.

19. An apparatus in accordance with claim 14, wherein at least one of said respective known signals that stimulate a respective first end of a respective net of interest comprises a square-wave pulse train and said signal correlation comprises auto-correlation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with itself.

20. An apparatus in accordance with claim 14, wherein said known signal comprises a square-wave pulse train and said signal correlation comprises cross-correlation of said digital representation of said digital representation of said capacitively coupled signal detected on said respective second end of said respective net of interest with an expected digital signature of said square-wave pulse train.

21. An apparatus in accordance with claim 14, further comprising:

a memory for storing each said respective sensed signal.

22. An apparatus in accordance with claim 21, wherein each one or more sensing probes are operable to sequentially sense a respective signal from a respective second end of each of said nets of interest corresponding to said subset of said plurality of stimulating probes when said respective known signal applied to said respective stimulating probe stimulates said first end of said corresponding net of interest.

23. A method for testing electrical integrity of a net of interest on a printed circuit board, said net of interest beginning at a first node and ending on a second node, said method comprising:

stimulating said first node with a known signal;

capacitively sensing a signal on said second node;

correlating said capacitively coupled signal with said known signal based only on said capacitively coupled signal and an expected digital signature of said known signal.

24. A method in accordance with claim 23, further comprising:

determining whether the level of correlation meets a pre-determined level of correlation.

25. A method for testing electrical integrity of nodes of interest on a printed circuit board, said method comprising:

for each of a plurality of nodes of interest on said printed circuit board:

stimulating said node of interest with a known signal;

capacitively sensing a signal on said node of interest; and

correlating said sensed signal with said known signal; and

determining whether the level of correlation meets a pre-determined level of correlation.

26. A method in accordance with claim 25, wherein:

said steps for stimulating said node of interest with a known signal and for capacitively sensing a signal on said node of interest are performed in parallel.

27. A method in accordance with claim 26, wherein:

said steps for stimulating said node of interest with a known signal and for capacitively sensing a signal on said node of interest are performed sequentially.

28. A method in accordance with claim 27, further comprising the step of:

for each of a plurality of nodes of interest on said printed circuit board:

storing said sensed signal in a memory associated with said node of interest.